REMARKS

Receipt of the Office action of February 13, 2006 is hereby acknowledged. In that action the Examiner: 1) rejected claim 3 as allegedly indefinite; 2) rejected claims 1, 7-10 and 13 as allegedly anticipated by Gee et al. (U.S. Pat. No. 6,317,872); 3) rejected claims 10-12, 14, and 22-23 as allegedly anticipated by Zaidi (U.S. Pat. No. 6,581,154); 4) rejected claims 18 and 21 as allegedly anticipated by Seal et al. (U.S. Pat. No. 6,965,984); 5) rejected claims 2-4 as allegedly unpatentable over Gee in view of Seal; 6) rejected claims 5-6 as allegedly unpatentable over Gee in view of Zaidi; 7) rejected claims 15-17 as allegedly unpatentable over Gee in view of Greenberger et al. (U.S. Pat. No. 6,092,179); rejected claims 16-17 as allegedly unpatentable over Gee in view of Greenberger in further view of Zaidi; 8) rejected claims 18-20 as allegedly unpatentable over Gee in view of Seal; 9) objected to the drawings; 10) objected to the specification; and 11) objected to claim 3.

With this Response, Applicants amend claims 1, 6, 14, and 15. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. AMENDMENTS TO THE SPECIFICATION

With respect to paragraphs [0001], [0014], [0023]-[0024], [0026]-[0028], [0030], and [0033], Applicants present a plurality of amendments to add serial numbers and/or patent numbers of related cases, and to correct grammatical shortcomings. Applicants also add paragraphs to address the drawing objections, discussed immediately below. No new matter is added.

II. DRAWING OBJECTIONS

The Office action objects to the drawings for various informalities. To address these concerns, Applicants present Figures 6A and 6B, as well as corresponding paragraphs [0011.1], [0011.2], [0034.1] and [0034.2]. As for Figure 6A and paragraph [0034.1], the figure and paragraph find support in the original disclosure at claims 2-4, as well as the original specification paragraphs [0020], [0026], [0028], and [0029]. As for Figure 6B and paragraph [0034.2], the figure and paragraph find support in the original

disclosure at claims 3 and 4, as well as the original specification paragraphs [0026] and [0028]. No new matter is added.

III. CLAIM OBJECTIONS

The Office action objects to claim 3 for various informalities. To address these concerns, Applicants present paragraph [0034.1]. Paragraph [0034.1] finds support in the original disclosure at claims 2-3, as well as the original specification paragraphs [0020], [0026], [0028], and [0029]. No new matter is added.

IV. 35 U.S.C. § 112, 2ND PARAGRAPH-BASED REJECTIONS

Claim 3 stands rejected as allegedly indefinite.

To address these concerns, Applicants present paragraph [0034.1]. Paragraph [0034.1] specifically recites "the information (*e.g.*, one or more indicators)", wherein the recitation finds support in the original disclosure at claim 2, as well as the original specification paragraph [0026]. The remainder of paragraph [0034.1] finds support in the original disclosure at claim 3, as well as the original specification paragraphs [0020], [0028], and [0029]. No new matter is added.

V. ART-BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Gee. Applicants amend claim 1 to more clearly define over Gee's switching between a program counter and a microprogram counter. The amendment finds support in the original specification at Paragraphs [0020] and [0030].

Gee is directed to real time processor optimized for executing Java programs. (Gee Title). In particular, Gee appears to disclose a JAVA embedded microprocessor (JEM) (Gee Col. 8, lines 35-36) comprising a program counter for accessing sequential bytecodes from the external memory (Gee Fig. 2 Elements 204 and 250; Col. 10, lines 46-53) and a microprogram counter for addressing and sequentially executing microinstructions (Gee Fig. 2 Element 226; Col. 9, lines 26-29). Gee teaches that **each** bytecode is interpreted as a pointer to a sequence of microinstructions which will actually be executed in place of the bytecode. (Gee Col. 8, lines 57-59). Thus, Gee teaches that for **each** bytecode retrieved by way of the program counter, the bytecode itself will not be

executed, but rather, the microinstructions will be executed by way of the microprogram counter.

Claim 1, by contrast, specifically recites, "wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters **based on a micro-sequence-active bit**." Applicants respectfully submit that Gee does not expressly or inherently teach such a system. Gee teaches execution of a microprogam for **each** bytecode retrieved. Gee is silent as to direct execution of the bytecode. Gee further teaches that for **each** bytecode, execution begins with the translation of the "opcode" portion of the bytecode into a starting microprogram address followed by execution of the microinstructions by the microsequencer (Gee Col. 8, lines 65-67 and Col. 9, lines 1-4). However, Gee fails to expressly or inherently teach a processor "wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters **based on a micro-sequence-active bit**."

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-9), should be allowed.

B. Claim 10

Claim 10 stands rejected as allegedly anticipated by Gee. Applicants respectfully traverse.

Claim 10 recites "Determining whether said instruction is to be executed or replaced by a group of other instructions." Applicants submit that the portion of Gee cited by the Examiner (Gee Fig. 2 Element 200; Col. 9, lines 5-52) does not expressly or inherently teach such a method. The Office Action relies on Gee's control-store receiving an address from the selector, wherein the selector provides the address from one of a plurality of sources. The reliance is misplaced. Gee teaches that **each** bytecode is interpreted as a pointer to a sequence of microinstructions which will actually be executed in place of the bytecode. (Gee Col. 8, lines 57-59). Thus, Gee teaches that for **each** bytecode retrieved by way of the program counter, the bytecode itself will not be executed, but rather, the microinstructions will be executed by way of the microprogram

counter. Gee is silent as to determining whether or not to execute the fetched instruction. Gee teaches that instruction bytecodes are fetched from code memory and execution begins with the translation of the "opcode" portion of the bytecode into a starting microprogram address for further execution by the microsequencer (that comprises the selector) (Gee Col. 8, lines 63-67). Therefore, Applicants respectfully submit that the cited reference does not expressly or inherently teach "Determining whether said instruction is to be executed or replaced by a group of other instructions."

Claim 10 also stands rejected as allegedly anticipated by Zaidi. Applicants respectfully traverse.

Zaidi is directed to expanding microcode associated with full and partial width macroinstructions. (Zaidi Title). In particular, Zaidi appears to disclose a computer for dynamically expanding and executing microcode routines utilizing a multi-level decoder (Zaidi Col. 2, lines 36-37). Zaidi teaches that the instruction decoder (comprising a micro-instruction sequencer; Zaidi Fig. 2 Element 200) converts a macro-instruction into one or more packed or scalar Uops (Zaidi Col. 3, lines 54-56). In particular, Zaidi teaches that **each** macro-instruction received by the micro-instruction sequencer is transformed into one or more Uops and/or SUops (Zaidi col. 3, lines 57-60). Thus, Zaidi teaches that the received macro-instructions are not directly executed, but rather, the macro-instructions are transformed for execution as one or more Uops and/or SUops.

Claim 10 recites "Determining whether said instruction is to be executed or replaced by a group of other instructions." Applicants submit that the portion of Zaidi cited by the Examiner (Zaidi Fig. 2 Element 203; Col. 3, lines 55-67 and Col. 4, lines 1-7) does not expressly or inherently teach such a method. The Office Action relies on Zaidi's micro-instruction sequencer logic that determines if the instruction is a Uop or a SUop that will further be expanded and replaced by a group of instructions. The reliance is misplaced. Zaidi teaches that **each** macro-instruction received by the micro-instruction sequencer is transformed into one or more Uops and/or SUops (Zaidi col. 3, lines 57-60). However, Zaidi is silent as to direct execution of the retrieved macro-instructions. Therefore, Applicants respectfully submit that the cited reference does not expressly or inherently

teach "Determining whether said instruction is to be executed or replaced by a group of other instructions."

Based on the foregoing, Applicants respectfully submit that claim 10, and all claims which depend from claim 10 (claims 11-14), should be allowed.

C. Claim 15

Claim 15 stands rejected as allegedly unpatentable over Gee in view of Greenberger. Applicants amend claim 15 to more clearly define over Gee's switching between a program counter and a microprogram counter. The amendment finds support in the original specification at Paragraphs [0020] and [0030].

Gee is directed to real time processor optimized for executing Java programs. (Gee Title). In particular, Gee appears to disclose a JAVA embedded microprocessor (JEM) (Gee Col. 8, lines 35-36) comprising a program counter for accessing sequential bytecodes from the external memory (Gee Fig. 2 Elements 204 and 250; Col. 10, lines 46-53) and a microprogram counter for addressing and sequentially executing microinstructions (Gee Fig. 2 Element 226; Col. 9, lines 26-29). Gee teaches that **each** bytecode is interpreted as a pointer to a sequence of microinstructions which will actually be executed in place of the bytecode. (Gee Col. 8, lines 57-59). Thus, Gee teaches that for **each** bytecode retrieved by way of the program counter, the bytecode itself will not be executed, but rather, the microinstructions will be executed by way of the microprogram counter. Greenberger is directed to core processor with customizable function unit. (Greenberger Title).

Claim 15, by contrast, specifically recites, "wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters **based on a micro-sequence-active bit**." Gee teaches execution of a microprogam for **each** bytecode retrieved. Gee is silent as to direct execution of the bytecode. Gee further teaches that for **each** bytecode, execution begins with the translation of the "opcode" portion of the bytecode into a starting microprogram address followed by execution of the microinstructions by the microsequencer (Gee Col. 8, lines 65-67 and Col. 9, lines 1-4). Thus, even if the teachings of Greenberger are precisely as the Office Action suggests (which Applicants

do not admit), Gee and Greenberger still fail to teach or suggest a "wherein an instruction is replaced by a micro-sequence comprising one or more instructions and the active program counter switches between the first and second program counters **based on a micro-sequence-active bit**."

Based on the foregoing, Applicants respectfully submit that claim 15, and all claims which depend from claim 15 (claims 16-17), should be allowed.

D. Claim 18

Claim 18 stands rejected as allegedly anticipated by Seal and as allegedly unpatentable over Gee in view of Seal. Applicants respectfully traverse.

Seal is directed to data processing using multiple instruction sets (Seal Title). In particular, Seal appears to disclose data processing system comprising bytecode translation hardware (Seal Col. 5, lines 60-62). Seal teaches that the bytecode translation hardware serves to generate a sequence of corresponding ARM instructions (Seal Col. 6, lines 10-15). Seal further teaches that when the bytecode translation hardware is inactive/unavailable or when non-hardware supported bytecodes are encountered, the bytecodes are referred to a software instruction interpreter (Seal Col. 6, lines 29-50). In particular, Seal teaches that the software instruction interpreter provides for fragments of code (comprising ARM native instructions) to be executed in place of bytecodes that are not supported by translation hardware, wherein the fragments of code to be executed are identified by performing a lookup within a table of pointers (Seal Col. 6, lines 51-67 and Col. 7, lines 1-6).

Claim 18 specifically recites "each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed". Applicants submit that the portion of Seal cited by the Examiner (Seal Fig. 2 Element 24; Col. 6, lines 60-67 and Col. 7, lines 1-23) does not expressly or inherently teach such an electronic device. The Office Action relies on Seal's table of pointers that point to code fragments that perform the processing specified by non-hardware supported bytecodes. (Seal Col. 6, lines 64-67). The reliance is misplaced. Seal teaches that **each** of a stream of Java bytecodes is to be executed (with possible intervening operand bytes). (Seal Col. 6, lines 53-55). However, Seal is silent as to each bytecode (i.e., each

instruction) having a corresponding indicator (i.e., the first field) indicating whether the bytecode is to be executed. Rather, Seal teaches that fragments of code (comprising ARM native instructions) are executed in place of bytecodes that are not supported by translation hardware, wherein the fragments of code to be executed are identified by performing a lookup within a table of pointers (Seal Col. 6, lines 60-67 and Col. 7, lines 1-6). However, the table of pointers does not indicate whether the bytecode is to be executed. Therefore, Applicants respectfully submit that the cited reference does not expressly or inherently teach "each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed".

Moreover, with regard to Gee, Gee teaches that **each** bytecode is interpreted as a pointer to a sequence of microinstructions which will actually be executed in place of the bytecode (Gee Col. 8, lines 57-59). Gee is silent as to determining whether or not to execute the fetched instruction. Therefore, even if the teachings of Gee are considered with Seal, Gee and Seal still fail to teach or suggest an electronic device comprising "each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed".

Based on the foregoing, Applicants respectfully submit that claim 18, and all claims which depend from claim 18 (claims 19-21), should be allowed.

E. Claim 22

Claim 22 stands rejected as allegedly anticipated by Zaidi. Applicants respectfully traverse.

Claim 22 recites "a means for determining whether an instruction is to be executed or replaced by a micro-sequence of other instructions." Applicants submit that the portion of Zaidi cited by the Examiner (Zaidi Fig. 2 Element 203; Col. 3, lines 55-67 and Col. 4, lines 1-7) does not expressly or inherently teach such a processor. The Office Action relies on Zaidi's micro-instruction sequencer logic that determines if the instruction is a Uop or a SUop that will further be expanded and replaced by a group of instructions. The reliance is misplaced. Zaidi teaches that **each** macro-instruction received by the micro-instruction sequencer is transformed into one or more Uops and/or SUops (Zaidi col. 3, lines 57-60). However, Zaidi is silent as to direct execution of the retrieved macro-

instructions. Therefore, Applicants respectfully submit that the cited reference does not accomplish its intended purpose of anticipating claim 22.

Based on the foregoing, Applicants respectfully submit that claim 22, and all claims which depend from claim 22 (claim 23), should be allowed.

VI. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

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Amendments to the Drawings:

Applicants submit a new sheet comprising Figures 6A and 6B. No new matter is added.

Attachment: New Sheet